

Atty Docket No.: JCLA12709

Serial No.: 10/823,489

REMARKS

Claims 1, 10-13, 15, 16-18, 19, 20, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Patent No.6,771,052) in view of Giannopoulos (U.S. Patent No.6,549,432). Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Patent No.6,771,052) in view of Giannopoulos (U.S. Patent No.6,549,432) in further view of Huang (U.S. Patent No.6,344,979). Moreover, claims 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Patent No.6,771,052) in view of Giannopoulos (U.S. Patent No.6,549,432) in further view of Crine (U.S. Patent No. 5, 400, 239). Applicant respectfully traverses the preceding rejections based on the following arguments and reconsideration of this application is respectfully requested.

Atty Docket No.: JCLA12709

Serial No.: 10/823,489

Discussion of rejection to claims under 35 U.S.C. §103(a)

Claims 1, 10-13, 15, 16-18, 19, 20, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Patent No.6,771,052) in view of Giannopoulos (U.S. Patent No.6,549,432).

In response thereto, applicant respectfully traverses the rejection based on the following arguments. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine references teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teachings or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir.1991). The Examiner alleged that it would be obvious to the artisan at the time of the invention to include the use of a first capacitor and controller seen in Giannopoulos to synchronously control the time delay between the front-end converter and a pulse supplied to a first and second converter arrangement in order to provide soft switching (Giannopoulos col.2, lines 30-35). However, col.2, lines 30-35 in Giannopoulos

Atty Docket No.: JCLA12709

Serial No.: 10/823,489

only discloses a flyback converter with a capability of soft switching of input switch. Furthermore, from col.4, lines 18-21 and Fig.6, in Giannopoulos, a controller 530 is used to control the switching positions of switching devices S1, S2, i.e. **the turn-on sequence of the switching devices** so that the voltage across input switching device S_0 is driven to zero at the end of the switching cycle, whereby when switching device S_0 is turned on at beginning of the following switching cycle, zero-voltage switching is achieved. **In other words, the controller 530 cannot function to control the claimed delay time between the timing of input capacitor of front-end converter and timing of the first and second buck converters.** As such, the controller 530 is obviously not identical to "a time delay synchronous control circuit" as claimed in claims 1 and 15 because the controller 530 is incapable of "controlling a delay time between the time the front-end converter begins to have a pulse current to the first output capacitor and the time the first buck converter and the second buck converter being turned on is adjusted" as claimed in claims 1 and 18. Likewise, the controller 530 is incapable of "controlling the first buck converter and the second buck converter alternatively drawing one of the two pulse currents from the first output capacitor during the time when every two pulse of the output current of the front-end converter are provided," as claimed in claim 15.

Atty Docket No.: JCLA12709

Serial No.: 10/823,489

Furthermore, as can be seen from timing chart of I_{prim} shown in Fig.6, in Giannopoulos, I_{prim} (i.e. output current from output capacitor V_{in} of the front-end converter 502) is not affected by post converters 517, 519 and 515 that are respectively coupled to secondary winding n_s of transformer 506. This is because, during $T_{off,0}$ in switching time T_{per} , the I_{prim} is kept zero. In other words, in Giannopoulos, I_{prim} is not drawn by post converters, which means Giannopoulos fails to disclose a limitation of "the first buck converter and the second buck converter draw pulse current from the first output capacitor during the time when the front-end converter has the pulse output current to the first output capacitor," as claimed in claim 1. As such, Giannopoulos is not able to achieve a purpose of reducing ripple current on the output capacitor of the front-end converter as disclosed in paragraph [0007] in the specification. Hence, even if Ostojic and Giannopoulos could be combined, this combination still fails to teach, suggest or disclose the aforementioned limitation.

Additionally, the functionality of reducing power dissipated by input capacitor of the front-end converter (see lines 8-9 in paragraph [0004] in specification of the invention) is not addressed at all in either of Ostojic and Giannopoulos. Thus, even if Ostojic and Giannopoulos could be combined, this combination still fails to teach, suggest or disclose "controlling a delay time between the time the front-end converter begins to have a pulse current to the first

Atty Docket No.: JCLA12709

Serial No.: 10/823,489

output capacitor and the time the first buck converter and the second buck converter being turned on is adjusted" as claimed in claims 1,18, and "controlling the first buck converter and the second buck converter alternatively drawing one of the two pulse currents from the first output capacitor during the time when every two pulse of the output current of the front-end converter are provided," as claimed in claim 15. Moreover, the feature of "the buck switch begins to turn on synchronously with the rectifier at the time the converter turns off and turn off at the time before the time when the converter turns on," as claimed in claim 22, is also not disclosed in the combination of Ostojic and Giannopoulos. Accordingly, the independent claims 1, 15, 18 and 22 are not rendered obvious by Ostojic and in view of Giannopoulos, and thus patentable.

Regarding dependent claims 10-13, 16-17, 19-20 and 21-24, they should be patentable for the reason that they contain all limitations of their respective patentable base independent claims 1, 15, 18 and 22.

Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Patent No.6,771,052) in view of Giannopoulos (U.S. Patent No.6,549,432) in further view of Huang (U.S. Patent No.6,344,979)

Page 6 of 8

Atty Docket No.: JCLA12709

Serial No.: 10/823,489

Claims 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Patent No.6,771,052) in view of Giannopoulos (U.S. Patent No.6,549,432) in further view of Crine (U.S. Patent No. 5, 400, 239).

In response thereto, applicant respectfully traverses the rejections based on the following arguments. By the same argument to claims 10-13, 16-17, 19-20 and 21-24, as claims 2-9, 14 and 21 are dependent claims, they should be patentable for the reason that they contain all limitations of their respective patentable base independent claims 1 and 18.

Atty Docket No.: JCLA12709

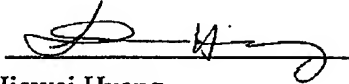
Serial No.: 10/823,489

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-24 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 2/16/2007



Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949)-660-0809